WHAT IS CLAIMED IS:

1. A method for evaluating reliability of a semiconductor chip, comprising the steps of:

determining strain at a location in a structure;

evaluating failures in a plurality of the structures after stress cycling to determine a strain threshold with respect to a feature characteristic; and

evaluating structures on a chip based on the feature characteristic to predict reliability based on the strain threshold and the feature characteristic.

2. The method as recited in claim 1, wherein the feature characteristic includes a liner thickness formed in via holes and the step of evaluating structures on a chip based on the feature characteristic to predict reliability includes measuring a thickness of a liner to predict electrical failures.

3. The method as recited in claim 1, wherein the step of evaluating failures in a plurality of the

structures includes the step of thermal cycling the plurality of structures.

4. The method as recited in claim 1, wherein the step of determining strain at a location in a structure includes determining strain at a bottom of a via in contact with a liner in the via.

5. The method as recited in claim 1, wherein the step of evaluating failures in a plurality of the structures includes the step of determining the strain threshold such that below the threshold no failures occur in the structures.

6. The method as recited in claim 1, wherein the strain is generated by thermal mismatch and the method further comprises the step of altering geometry of the feature characteristic to reduce strain.

7. The method as recited in claim 6, wherein the

step of altering includes altering a thickness of a via liner.

8. The method as recited in claim 1, wherein the strain is generated by thermal mismatch and the method further comprises the step of altering material selection of the feature characteristic to reduce strain.

9. The method as recited in claim 8, wherein the thermal mismatch is greater than 30 ppm/°C between the feature characteristic and its surroundings.

10. A method for evaluating reliability of a semiconductor chip, comprising the steps of:

providing a semiconductor chip design having a metal structure therein, the metal structure being in contact with dielectric material;

determining strain at a location at or adjacent to the metal structure due to thermal stress;

evaluating failures in a plurality of the metal

structures to determine a strain threshold for failures;

correlating the strain threshold to characteristics of the metal structure; and

predicting reliability of semiconductor chips based upon measured characteristics of the metal structure.

11. The method as recited in claim 10, wherein the characteristics of the metal structure include a liner thickness formed in via holes and further comprising the step of measuring a thickness of a liner to predict electrical failures.

12. The method as recited in claim 10, wherein the step of evaluating failures includes the step of thermal cycling the plurality of metal structures.

13. The method as recited in claim 10, wherein the step of evaluating failures includes the step of determining the strain threshold such that below the threshold no failures occur in the structures.

14. The method as recited in claim 10, wherein the strain is generated by thermal mismatch and the method further comprises the step of altering geometry or material selection of the metal structures to reduce strain.

15. The method as recited in claim 14, wherein the mismatch between the metal structure and the dielectric is greater than 30 ppm/°C.

16. A semiconductor device, comprising:

a metallization structure having a metal patterned with conductive liners along bottoms and sidewalls of vias of the structure;

a dielectric material surrounding the metal, wherein a mismatch in coefficient of thermal expansion (CTE) exists between the metallization and surrounding insulator;

the conductive liners being configured and dimensioned to provide a liner thickness that makes the metallization structure less susceptible to thermal cycle failure such

that no failures are expected during thermal cycle stress conditions.

17. The device as recited in claim 16, wherein the metal includes copper (Cu), the conductive liner material includes tantalum (Ta).

18. The device as recited in claim 17, wherein the liner thickness is in the range of between about 25nm and about 35nm and the CTE of the insulator is in the range of between about 50ppm/°C and about 75ppm/°C.

19. The device as recited in claim 17, wherein the liner thickness is in the range of between about 35nm and about 45nm and the CTE of the insulator is in the range of between about 75ppm/°C and about 100ppm/°C.

20. The device as recited in claim 16, wherein the metal includes copper (Cu), the conductive liner material includes titanium (Ti).

21. The device as recited in claim 20, wherein the liner thickness is in the range of between about 35nm and about 55nm and the CTE of the insulator is in the range of between about 75ppm/°C and about 100ppm/°C.

22. The device as recited in claim 16, wherein the metal includes copper (Cu), the conductive liner material includes tungsten (W).

23. The device as recited in claim 22, wherein the liner thickness is in the range of between about 10nm and about 20nm and the CTE of the insulator is in the range of between about 50ppm/°C and about 75ppm/°C.

24. The device as recited in claim 22, wherein the liner thickness is in the range of between about 20nm and about 30nm and the CTE of the insulator is in the range of between about 75ppm/°C and about 100ppm/°C.

25. The device as recited in claim 16, wherein the metal includes aluminum (Al), the conductive liner material includes titanium (Ti).

26. The device as recited in claim 25, wherein the liner thickness is in the range of between about 25nm and about 35nm and the CTE of the insulator is in the range of between about 50ppm/°C and about 75ppm/°C.

27. The device as recited in claim 25, wherein the liner thickness is in the range of between about 35nm and about 55nm and the CTE of the insulator is in the range of between about 75ppm/°C and about 100ppm/°C.

28. The device as recited in claim 16, wherein the metal includes aluminum (Al), the conductive liner material includes tungsten (W).

29. The device as recited in claim 28, wherein the liner thickness is in the range of between about 10nm and

about 20nm and the CTE of the insulator is in the range of between about 50ppm/°C and about 75ppm/°C.

30. The device as recited in claim 28, wherein the liner thickness is in the range of between about 20nm and about 30nm and the CTE of the insulator is in the range of between about 75ppm/°C and about 100ppm/°C.